REMARKS

The Application has been carefully reviewed in light of the Office Action dated February 20, 2004 (Paper No. 9). Claims 1 to 18 are in the application, of which Claims 1, 11, 17 and 18 are the independent claims. Claims 1 to 3, 11 and 17 are being amended. Reconsideration and further examination are respectfully requested.

Initially, Applicant gratefully acknowledges the indication that Claims 17 and 18 recite patentable subject matter. Claim 17 is amended herein to correct a typographical error, and such amendment is not seen to impact the allowed status of the claim.

Claims 1 to 8, 11, 12, 15 and 16 have been rejected under 35 U.S.C. §103(a) over U.S. Patent 5,357,152 (Jennings) and U.S. Patent 6,112,019 (Chamdani). Reconsideration and withdrawal of the rejection are respectfully requested for the reasons set forth below.

The present invention generally concerns a computer processor comprising a plurality of processing units interconnected via a communication means. An important feature of the present invention is that the communication means which interconnect the plurality of processing units is includes a common bus, over which packetized information may be communicated. In a first configuration arranged by the communication means, the processing unit may have a larger number of the processing units arranged in parallel than in a second configuration also arranged by the dynamically-configurable communication means, and the second configuration may have a deeper pipeline depth than the first configuration.

By virtue of this arrangement, communication paths for packetized information between the processing units can be selectively arranged to suit the nature of the processing, such that has the requirements of processing change, the configuration of the processing units can be adapted to suit the changing requirements.

Turning to the specific language of the claims, Claim 1 defines a computer processor comprising a plurality of processing units interconnected for communication of packetized information over a common bus of a communication means. The communication means is dynamically configurable based on a processing of a computer program to thereby selectively arrange communication paths for the packetized information between the processing units in at least first and second distinct configurations, the first distinct configuration having a larger number of the processing units arranged in parallel than the second distinct configuration, and the second distinct configuration having a deeper pipeline depth than the first distinct configuration.

The applied art, namely Jennings and Chamdani, are not seen to disclose or to suggest the above features, particularly as regards a communication means dynamically configurable based on a processing of a computer program to selectively arrange communication paths for packetized information between the plurality of processing units over a common bus in at least two distinct configurations.

Jennings is seen to describe a system having the logic network has a fixed logic networks, as shown in Figures 3 and 4, for communicating logic function selection signals, as shown in Figures 3 and 4. More particularly, Jennings is seen to describe a fixed logic network which is not able to be varied once set. Jennings is not seen to

describe communication of packetized information between processing units over a common bus.

More particularly, Jennings is seen to describe a logic network configuration capable of performing a set of fixed functions, and a programmable circuit, which provides a first signal that selects a desired logic function from the set of fixed functions that is to be performed by the logic network, and a second signal that controls the operation of the selected logic function so as to initiate, advance and terminate the selected function. As is described in Jennings, the first signal identifies an operation such as a counter operation, and the second signal initiates, advances and terminates the count operation. (Jennings, Abstract and col. 1, line 42 to col. 2, line 34.)

As they are understood, the cited portions of Jennings are seen to describe that the programmable circuit can be programmed to control a fixed-configuration logic network to perform operations from the set of operations provided by the logic network, such that the programmable circuit is programmed to provide the first and second control signals to select from the set of fixed operations and to initiate the selected operation(s). This is not seen to be the same as a communication means which is dynamically configurable to selectively arrange communication paths for packetized information between the plurality of processing units over a common bus in at least two distinct configurations.

Chamdani is not seen to remedy the deficiencies noted with respect to Jennings. More particularly, and while Chamdani describes pipelines of different sizes, Chamdani is not seen to disclose or to suggest an arrangement by which a communication

means is configurable to interconnect a plurality of processing units so as to arrange the processing units in at least two distinct configurations. The cited portion of Chamdani, i.e., col. 32, lines 19 to 38, is seen to describe a fixed processor configuration, which is not seen to in any way provide for dynamic configuration of a communication means to selectively arrange processing units in different and distinct configurations. Nothing in the cited portion of Chamdani is seen to disclose or to suggest a communication means dynamically configurable to selectively arrange communication paths for packetized information between the plurality of processing units over a common bus in at least two distinct configurations.

Therefore, for at least the foregoing reasons, Claim 1 is believed to be in condition for allowance.

Claim 11 defines data processing method using a computer processor having a plurality of processing units interconnected by communication means comprising a step of dynamically configuring the communication means according to a processing of a computer program to thereby selectively arrange the processing units in a plurality of configurations having a different number of said processing units arranged in parallel and a different number of said processing units arranged in pipelined layers.

Based on the above discussion, the applied art, namely Jennings and Chamdani, is not seen to disclose or to suggest dynamically configuring a communication means to selectively arrange communication paths for packetized information, over a common bus of the communication means, between a plurality of processing units in a plurality of configurations having a different number of the processing units arranged in

parallel and a different number of the processing units arranged in pipelined layers.

Therefore, for at least the foregoing reasons, Claim 11 is believed to be in condition for allowance.

The remaining claims are each dependent from the independent claims discussed above and are therefore believed patentable for the same reasons. Because each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing, the entire application is believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office by telephone at (714) 540-8700. All correspondence should be directed to our address given below.

Respectfully submitted,

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